What does Cadence provide for OpenVX?
Cadence Tensilica Processor and DSP IP Business Unit

TENSILICA CUSTOMERS

4B+ Processors Shipping Annually

DSP LICENSING REVENUE

#1 DSP IP Licensing Revenue

TENSILICA LICENSEES

LEADING AUDIO DSP IP

TOP Audio DSP Choice

GLOBAL ECOSYSTEM

200+ Ecosystem Partners

SEMICONDUCTORS

17 of the Top 20 Semiconductor Vendors Use Tensilica
Cadence Application Programming Kit (APK) includes:

• Front end: the OpenVX API, compliant to OpenVX 1.1
  – Calling any OpenVX API invokes the API “front end” module

• Graph Mapper: Translates OpenVX graph to a “script” that can run on Vision DSPs
  – Is invoked by graph verification, usually via vxVerifyGraph, but sometimes also indirectly via vxProcessGraph or vxScheduleGraph
  – Determines kernels to use, tile sizes, memory requirements, etc.

• Runtime: executes scripts
  – Invoked by vxProcessGraph or vxScheduleGraph
  – Launches optimized kernels on the Vision DSP
  – Handles DMA, kernel execution, notification of completion for vxWaitGraph

• XI Library: executes kernels
  – Highly optimized kernels for OpenVX functions
Cadence Vision P6 DSP

Instruction issue overhead amortized over hundreds of ALU ops per cycle

5 VLIW slots

Timers, Intervalots, Performance Counters

Power Management

Pipeline Management

Instruction Decoder

Instruction Memory 1 128

Instruction Memory 2 128

Instruction Cache 128

Scalar Processing Units

Scalar Register File

Optional VFP (with FP16)

Cache Controller

Data Memory 0

Bank 1 512

Bank 0 512

Data Memory 1

Bank 1 512

Bank 0 512

Memory Mux

SuperGather Technology

Load

Load/Store

Custom Instructions

Vector Register File (32)

Accumulator Register File (4)

Predicate Register File

Enhanced Vector Processing Units

- 256 MACs
- Processes 9728 bits per cycle
- Enhanced instruction set
- Smart instruction slotting

ON-the-fly data reorganization within vectors

Build-in 3D DMA

2x512 vector load/store

32x16 “SuperGather”

AXI4 Interface

128

Dual bus interfaces

AXI4

128

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Cadence OpenVX block diagram (dual core)

Host
(e.g., Xtensa controller or Other CPU)

User Program

OpenVX API

vxVerifyGraph
vxProcessGraph

Graph Mapper

binary script

Host Runtime

IPC Driver

OS (e.g. Linux)

Vision DSP
(e.g. P5/P6)

Legend

APK Component

Legend

APK Component

IPC Runtime

DMA Library

XI Library

Shared memory
Cadence OpenVX

• Fully compliant to OpenVX 1.1
• Highly optimized kernels leveraging the Cadence XI Library
  – Performance benchmarks provided
• Automatic tiling, DMA, local memory management, scatter-gather kernels
  – Via provided Graph Mapper and Runtime
• Automatic overlapping of data transfer (DMA) and compute
• Supported on Tensilica Vision P5 and Vision P6 processor cores
  – Compliance tested for 2-core system with Xtensa host running Linux 4.3 connected to Vision DSP
• Vision DSP IP license includes source code for all APK modules
Example Application

• Sparse optical flow:
  – Harris corners → Gaussian pyramid construction → Pyramidal LKT tracking

• From the Khronos OpenVX tutorial materials
  – Graph runs unmodified on Cadence APK 4.0 (replaced OpenCV video I/O functions)

• In video frames below, pedestrians walk through a scene
  – Red dots are detected features; yellow arrows indicate features tracked from previous frame

Source: [http://www.cvg.reading.ac.uk/PETS2009/a.html](http://www.cvg.reading.ac.uk/PETS2009/a.html)
Deliverables

• A single core bare metal (no OS) workspace
  – An Xtensa Xplorer workspace (apk4_vision_ovx_package.xws)
  – Enables quick start up and efficient simulation on DSP
  – A good workspace to start with and become familiarize with OpenVX

• A Dual core (Host and DSP) workspace with Linux on Host
  – Delivered as a gzipped tar archive file (openvx-linux-apk-4.0.tar.gz)
  – Simulates a separate controller to run the “host” and Vision DSP executes the graph
  – A good workspace which will be closer to real deployment system

• A folder with all the test input images for Optical_Flow_Test example
• Release Notes